We Claim:

1. An integrated memory circuit, comprising:

a memory cell array;

a test circuit connected to said memory cell array, said test circuit generating an assessment datum, the assessment datum being dependent on a result of a comparison between a datum read from said memory cell array and a datum previously written to said memory cell array; and

a coding unit coupled to said test circuit for coding a plurality of assessment data to form a coded test signal, the coded test signal being a voltage signal representing the plurality of assessment data and functioning as a coded test datum.

2. The integrated memory circuit according to claim 1, wherein said coding unit has a digital-to-analog converter circuit.

3. The integrated memory circuit according to claim 2, wherein said coding unit generates a plurality of voltage levels, so that a respective voltage level is assigned to a specific pattern of the plurality of assessment data.

4. The integrated memory circuit according to claim 1, further comprising an external terminal for reading the coded test datum from the integrated memory circuit.

5. The integrated memory circuit according to claim 4, wherein the voltage signal can be read out within a clock cycle.

6. A tester unit for receiving coded assessment data, comprising:

a decoding circuit for receiving a coded test signal containing a voltage signal which can assume a plurality of signal levels, said decoding circuit generating a respective pattern of assessment data in response to a voltage level of the voltage signal received.

7. The tester unit according to claim 6, wherein said decoding circuit has an analog/digital converter circuit.

8. A test system, comprising:

an integrated memory circuit, containing:

a memory cell array;

a test circuit connected to said memory cell array, said test circuit generating an assessment datum, the assessment datum being dependent on a result of a comparison between a datum read from said memory cell array and a datum previously written to said memory cell array; and

a coding unit coupled to said test circuit for coding a plurality of assessment data to form a coded test signal, the coded test signal being a voltage signal representing the plurality of assessment data and functioning as a coded test datum;

a tester unit connected to said integrated memory circuit so that the coded test datum can be transmitted to said tester unit.

9. The test system according to claim 8, wherein said tester unit contains a decoding circuit receiving the coded test signal containing the voltage signal which can assume a plurality of signal levels, said decoding circuit generating a respective pattern of assessment data in response to a voltage level of the voltage signal.

10. A method for testing an integrated memory circuit having a memory cell array, which comprises the steps of:

comparing a datum read from the memory cell array with a datum previously written to the memory cell array;

generating an assessment datum in dependence on a result of the comparing step;

coding a plurality of assessment data into a coded test datum;

transmitting the coded test datum to a tester unit; and

decoding the coded test datum back into the plurality of assessment data.

11. The method according to claim 10, which further comprises performing the coding of the assessment data such that the coded test datum can have one of a plurality of voltage levels, each of the voltage levels representing a specific pattern of assessment data.